Claims

We claim:

1. A scan test circuit design imbedded within an integrated circuit chip having a test clock signal, comprising:

at least one scan-in terminal coupled to receive a test stimulus input data;

at least one scan-out terminal to output testing resultant data;

at least one scan chain group each having a clock domain, the at least one scan chain group coupled between one of the at least one scan-in terminal and one of the at least one scan–out terminal, wherein the test clock signal enables the testing of each of the at least one scan chain group, each scan chain group has a corresponding test mode signal to shift the test stimulus input data at a shift clock rate derived from the corresponding clock domain, wherein each at least one scan chain group comprises,

a demultiplexer unit, having an input, an enable input, a first output and a second output, the input coupled to receive the test stimulus input data, the enable input coupled to receive the test clock signal, the first output coupled to a functional input for the portion of the integrated circuit chip being tested,

a first multiplexer unit, having a first input, a second input, an enable input, and an output, the first input coupled to the second output of the demultiplexer unit, the enable input coupled to receive a simultaneous test mode signal,

a scan chain, having an input, a control input, and an output, the input coupled to the output of the first multiplexer unit, the scan chain having a corresponding scan chain clock domain at a predetermined frequency, and

a second multiplexer unit, having a first input, a second input, an enable input, and an output, the first input coupled to the output of the scan chain, the second input coupled to receive functional output data from the

portion of the integrated circuit chip being tested to supply testing resultant data at the output;

a controlling demultiplexer coupled to the second output of one demultiplexer unit and coupled to receive the simultaneous test mode signal and a plurality of test mode signals for each scan chain group to generate control signals to be coupled to the second input of each first multiplexer unit to control the concurrent shifting of the test stimulus input data into each scan chain at the predetermined frequency;

a clock control mechanism coupled to receive the test clock signal, a test mode select pin inputs, a scan enable signal, functional clock and enable signals corresponding to each of the at least one scan chain groups to generate a control signal for each scan chain, the plurality of test mode signals for each scan chain group and the simultaneous test mode signal,

wherein the clock control mechanism coupled to the control input of each scan chain of the at least one scan chain group to enable one scan chain to shift test stimulus input data when the scan enable signal is enabled and the test clock signal is enabled, the clock control mechanism coupled to each scan chain to enable simultaneous capture of each of the at least one scan chain group when the scan enable, the test clock, and the simultaneous test mode signals are enabled; and

a controlling multiplexer coupled to the output of each scan chain and coupled to receive each test mode signal to generate a control signal for the second multiplexer of the least significant of the at least one scan chain group.

2. An integrated circuit chip as recited in claim 1, wherein the clock control mechanism comprises:

a scan logic device coupled to receive a test clock and a scan enable signal to generate an enable signal that detects the rising edge on the scan enable signal and an enable signal that detects a rising or falling transition on the scan enable signal;

at least one clock generator for a respective one of the at least one scan chain groups coupled to receive both enable signals generated by the scan logic device, the test clock signal, the function enable and clocking signals corresponding to the at least one scan chain group to produce a clock signal for controlling the scan chain of the respective at least one scan chain group; and

a decode logic unit, having the test mode select pins, the decode logic unit coupled to each one of the at least one clock generators to provide a test mode delta signal, a VLCT mode signal, the test mode signals corresponding to each respective one of the at least one scan chain groups, and the simultaneous test mode signal for simultaneous testing of all scan chain groups.

3. An integrated circuit chip as recited in claim 2, wherein the scan logic device comprises:

a DQ flip-flop, having a clock input, a D-input and a Q-output, the clock input coupled to receive the test clock signal, the D-input coupled to receive the scan enable signal;

an inverter coupled to the Q-output;

an AND gate, having a first input, a second input, and an output, to generate at the output the enable signal that detects the rising edge on the scan enable signal, the first input coupled to receive the scan enable signal, the second input coupled to the inverter; and

a NOR gate, having a first input, a second input and an output, to generate at the output the enable signal that detects a rising or falling transition on the scan enable signal, the first input coupled to the Q-output, the second input coupled to receive the scan enable signal.

4. An integrated circuit chip as recited in claim 2, wherein the clock generator comprises:

a first inverter coupled to receive the VLCT mode signal;

a second inverter coupled to receive the enable signal that detects the rising edge on the scan enable signal;

a first AND gate coupled to the first inverter and the second inverter;

a first OR gate coupled to receive the enable signal that detects a rising or falling transition on the scan enable signal and the test mode delta signal;

a third inverter coupled to the first OR gate;

a second AND gate coupled to the third inverter and coupled to receive one of the test mode signals corresponding to each respective one of the at least one scan chain groups;

a second OR gate coupled to the first and second AND gates;

a first DQ flip-flop, having a D-input, an enable input and a Q-output, the D-input coupled to the second OR gate;

a fourth inverter, having an input and an output, the input coupled to receive the test clock signal, the output coupled to enable input of the first DQ flip-flop;

a third AND gate coupled to the Q-output of the first DQ flip-flop and coupled to receive the test clock signal;

a NOR gate coupled to the third AND gate and coupled to receive a polarity test clock signal;

a second DQ flip-flop, having a D-input, an enable input and a Q-output, the D-input coupled to the NOR gate;

a fourth inverter, having an input and an output, the input coupled to receive the functional clock signal corresponding to the at least one scan chain group, the output coupled to enable input of the second DQ flip-flop;

a fourth AND gate coupled to the Q-output of the second DQ flip-flop and coupled to receive the functional clock signal corresponding to the at least one scan chain group; and

a multiplexer unit, having a first input, a second input, a control input and an output, to provide the clock signal for controlling the scan chain of the respective at least one scan chain group, the first input coupled to the fourth AND gate, the second input coupled to receive the functional enable signal corresponding to the at least one scan chain group, the control input coupled to a test mode signal.

5. An integrated circuit chip as recited in claim 2, wherein the decode logic unit comprises:

a plurality of DQ flip-flops, each having a D-input, a Q-output, an inverted Q-output, and a clock input, each clock input coupled to receive the test clock signal, each D-input coupled to a respective test mode select pin;

a plurality of NOR gates, each having a first input, a second input and an output, each first input coupled to a respective test mode select pin, each second input coupled to a respective Q-output of the plurality of DQ flip-flops; and

a OR gate coupled to the output of each of the plurality of NOR gates to generate the test mode delta signal

a plurality of multi-input AND gates, each having a number of inputs corresponding to the number of DQ flip-flops and an output, each input coupled to a Q-output or an inverted Q-output in a specified pattern to generate intermediate signals for each test mode corresponding to the at least one scan chain group and to generate the simultaneous test mode signal for simultaneous testing of all scan chain groups;

a first inverter coupled to receive the first intermediate signal for a respective test mode corresponding to the at least one scan chain group;

a second inverter coupled to receive the second intermediate signal for a respective test mode corresponding to the at least one scan chain group;

a third inverter coupled to receive the third intermediate signal for a respective test mode corresponding to the at least one scan chain group

a first AND gate coupled to the first and second inverter to provide the test mode signal corresponding to the third scan chain group;

a second AND gate coupled to the first and third inverter to provide the test mode signal corresponding to the second scan chain group;

a third AND gate coupled to the second and third inverter to provide the test mode signal corresponding to the second scan chain group;

a OR gate coupled to the first, second and third AND gates to generate the VLCT mode signal.

6. A method for testing an integrated circuit chip having at least two clock domains at respective domain test clock rates corresponding to at least two scan chain groups, using a very low cost test (VLCT) platform -Automatic Test Pattern Generator (ATPG), comprising:

(a) clocking a test stimulus input data into each scan chain of each said clock domain sequentially by clocking the test stimulus input data into one scan chain and disabling the clocks of the other respective scan chain groups to hold these other respective scan chain groups static, clocking said test stimulus input data at a shift clock rate derived from at least one of said scan chain clock domains;

(b) capturing on all scan chain groups resultant data simultaneously at a predetermined frequency corresponding to one of the plurality of scan chain groups domain test clock rate;

(c) storing resultant data from one of the plurality of scan chain groups that corresponds with the predetermined frequency;

(d) repeating steps (a) – (c) at a corresponding frequency for each of the at least two scan chain groups.

7. A method for stuck-at fault testing an integrated circuit chip having at least two clock domains at respective domain test clock rates corresponding to at least two scan chain groups, using a very low cost test (VLCT) platform for a full device scan Automatic Test Pattern Generator (ATPG), comprising:

(a) applying test mode select code signal to a plurality of test mode select pins of a clock control mechanism for controlling the shift scan inputs of the at least two scan chain groups;

(b) shifting a test stimulus input data into each scan chain of each said clock domain sequentially by shifting the test stimulus input data into one scan chain and disabling the clocks of the other respective scan chain groups to hold these other respective scan chain groups static, shifting said test stimulus input data at a shift clock rate derived from at least one of said scan chain clock domains;

(c) capturing on all scan chain groups resultant data simultaneously at a predetermined frequency corresponding to one of the plurality of scan chain

groups domain test clock rate by applying two capture pulses separated by the twice the period of the corresponding domain test clock rate;

(d) storing resultant data from one of the plurality of scan chain groups that corresponds with the predetermined frequency;

(e) repeating steps (a) – (d) at a corresponding frequency for each of the at least two scan chain groups.

8. A method for at-speed transition fault testing an integrated circuit chip having at least two clock domains at respective domain test clock rates corresponding to at least two scan chain groups, using a very low cost test (VLCT) platform for a full device scan Automatic Test Pattern Generator (ATPG), comprising:

(a) applying test mode select code signal to a plurality of test mode select pins of a clock control mechanism for controlling the shift scan inputs of the at least two scan chain groups;

(b) clocking a test stimulus input data into each scan chain of each said clock domain sequentially by clocking the test stimulus input data into one scan chain and disabling the clocks of the other respective scan chain groups to hold these other respective scan chain groups static, clocking said test stimulus input data at a shift clock rate derived from at least one of said scan chain clock domains;

(c) capturing on all scan chain groups resultant data simultaneously at a predetermined frequency corresponding to one of the plurality of scan chain groups domain test clock rate by applying two capture pulses separated by the twice the period of the corresponding domain test clock rate;

(d) storing resultant data from one of the plurality of scan chain groups that corresponds with the predetermined frequency;

(e) repeating steps (a) – (d) at a corresponding frequency for each of the at least two scan chain groups.